九十四學年度電機系碩士在職專班試題卷

科目： 基礎電子學

應考時間：100 分鐘

選擇題 (每題 5 分)

1. 對一理想的電壓放大器而言，下列何者敘述有誤? (A) 輸入阻抗愈大愈佳 (B) 輸出阻抗愈大愈佳 (C) 電壓增益愈大愈佳 (D) 以上皆非。
2. 下列何者敘述有誤? (A) 共射極(common-emitter)放大器之電壓增益遠小於 1 (B) 共集極(common-collector or emitter follower)放大器有極大的輸出阻抗 (C)共基極放大器(common-base)之電流增益遠大於 1 (D) 以上皆非。
3. 對一 pn 二極體而言，下列何者敘述為真? (A) 順向電流隨溫度增加而增加 (B) 逆向電流隨溫度增加而減小 (C) 順向偏壓之介面電容(junction capacitance)小於逆向偏壓之介面電容 (D) 以上皆真。
4. 對一互補式金氧半電晶體反相器(CMOS inverter)而言，下列何者敘述有誤? (A) 由 n-MOSFET 與 p-MOSFET 共同組成 (B) 功率損耗較 nMOS inverter 大 (C) noise margin 較 nMOS inverter 大 (D) 以上皆非。
5. 對一金氧半電晶體(MOSFET)而言，下列何者敘述為真? (A) 為一四端點(four terminals)元件(B) enhancement-mode nMOSFET 之臨限電壓(threshold voltage, V_{th})大於 0 V (C) 在相同的元件結構與幾何大小下，nMOSFET 之電流高於 pMOSFET (D) 以上皆真。
6. 若將二個 pn 二極體串接如 Fig. 1，在何種偏壓條件下可表現出雙載子電晶體(BJT)的特性? (A) $V_{BE} > 0$ 且 $V_{BC} < 0$ (B) $V_{BE} < 0$ 且 $V_{BC} < 0$ (C) $V_{BE} > 0$ 且 $V_{BC} > 0$ (D) 以上皆非。

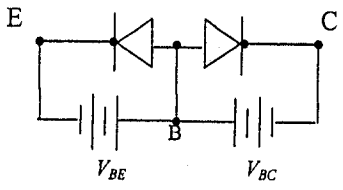

Fig. 1 Circuit for Problem 6.

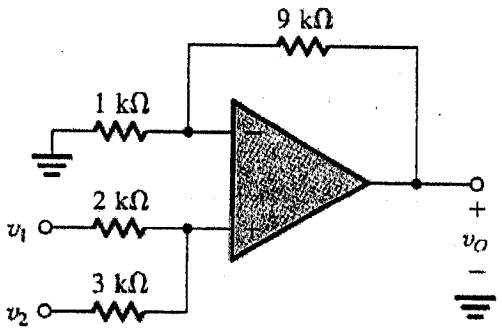

Fig. 2 Circuit for Problem 7.

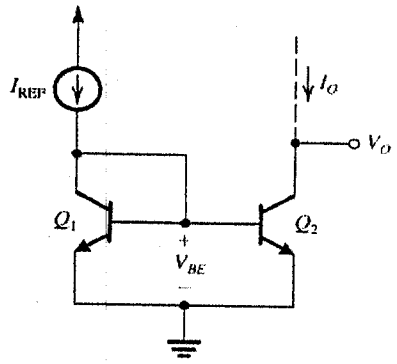

Fig. 3 Circuit for Problem 8

7. (16 分) Use the superposition principle to find the output voltage of the circuit shown in Fig. 2.

8. (16 分) Consider a BJT current mirror, as shown in Fig. 3, with a nominal current transfer ratio of unity. Let the transistors have $V_{BE} = 0.7$ V, $I_S = 10^{-15}$ A, $\beta = 100$, and $V_A = 100$ V. For $I_{REF} = 1$ mA, find I_O when $V_O = 5$ V. Also, find the output resistance.

9. (26 分)

For a dc voltage of 1 V applied to the input of the shown basic switched-capacitor integrator (Fig. 4) in which the $\phi 1$ and $\phi 2$ are 1 MHz two-phase nonoverlapping clock.

(a) (4 分) What charge is transferred for each clock cycle?

(b) (4 分) What is the average current drawn from the input source?

(c) (4 分) What is the equivalent resistance seen by the input source?

(d) (4 分) What change in output for each clock cycle? In what direction?

(e) (5 分) For an amplifier saturating at ± 10 V, how many cycles does it take for the amplifier output to go from one limit to the other?

(f) (5 分) What is the average slope of the output?

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10. (12 分) In usual applications of the shown logic circuit in Fig. 5, the signal C acts as a clock, being normally held high while X, Y and Z change. Finally, C falls while X, Y and Z are stable.
(a) (6 分) For signals having 0 V and 5 V levels and using positive logic convention, express F as a function of C, X,Y, Z.
(b) (6 分) For dynamic operation of the shown circuit equivalent to that of a basic symmetric inverter with $(W/L)_n$ = 4 μm/2μm and $(W/L)_p$ = 8μm/2μm, choose appropriate device widths, assuming that all device lengths are 2 μm.

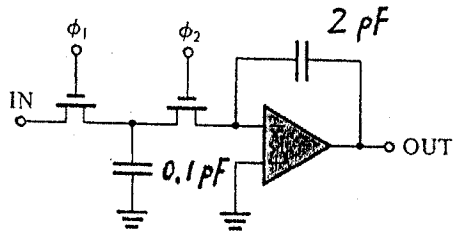

Fig. 4 Circuit for Problem 9.

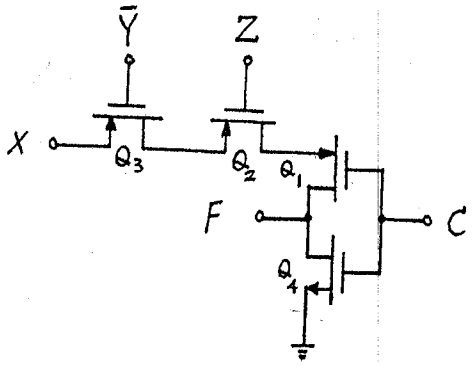

Fig. 5 Circuit for Problem 10.